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Power Quality Improvement using three-phase, three-Wire Self-supported DVR Based on SRF- theory

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Abstract—*The Dynamic Voltage Restorer (DVR) is one of the custom power devices which is used as active series compensator based on the principle of injecting voltage in series with the supply to address the voltage related power quality problems on supply side of the system such as voltage sag, voltage swell, voltage unbalance, harmonics etc. In this paper , three-phase, three-wire capacitor (self)-supported design of Voltage Source Converter(VSC) based DVR is proposed to mitigate sag, swell, unbalance, harmonics and their combinations in supply voltage. The desired results are achieved by using the control algorithm based on Synchronous Reference Frame Theory (SRFT). The synchronous reference frame theory is used here to generate reference load voltages. The load voltages are sensed and the errors between sensed load voltages and generated reference load voltages are used in Pulse Width Modulation (PWM) controller to generate gate pulses for VSC of the DVR. The modulation technique used is Sine-triangle based PWM (SPWM) technique. Besides this , two PI controllers are used in this system to regulate DC bus voltage and load voltage of the system. The proposed three-phase, three-wire capacitor (self)-supported DVR is simulated using MATLAB/SIMULINK software with simpowersystem toolbox. The simulation results obtained are demonstrated in this paper to verify the performance of the DVR, showing the compensation of about 15% sag and 15% swell with balanced as well as unbalanced supply voltage. Besides this, the harmonic compensation during sag as well as swell is also obtained*

1. INTRODUCTION

Power quality has become major issue in the performance of many industrial applications. Power quality studies show that from 80% to 90% of the customer's displeasure is due to voltage disturbances which are the most common power quality problems in modern distribution system, caused by substantial pollution and abnormal operating conditions[1, 2]. These power quality problems at point of common coupling (PCC) occur due to the voltage drop in feeders and transformers, various kinds of disturbances, faults, use of unbalanced lagging power factor consumer loads, and so on. These voltage-related power quality problems include voltage spikes, surges, flickers, sags, swells, notches, fluctuations, voltage imbalance, waveform distortion, and so on[2]. These disturbances can cause the malfunction of voltage-sensitive loads in factories, buildings, and hospitals etc. To address these voltage related power quality problems devices called active series compensators are used. These active series compensators are used to inject the voltage of required magnitude, and frequency in series with the distribution feeder to restore the voltage across the loads to protect the sensitive loads from these voltage related power quality problems. These compensators are also known as dynamic voltage restorers (DVRs)[3]. DVRs are mainly of three types based on the energy storage system used namely rectifier-supported DVR, battery-supported DVR, and capacitor-supported DVR. Besides this, many topologies and control methods have been presented for DVRs. In this work capacitor-supported DVR has been employed as this the most popular cost effective solution for protection of sensitive loads from supply-side voltage quality problems[3, 4]. Different control techniques are reported in the literature such as control techniques based on synchronous reference frame theory (SRFT), Adaline-based fundamental extraction, instantaneous symmetrical component theory, PQR instantaneous power theory etc. In this paper, a simple generalized control algorithm for self-supported DVR is developed based on the basic SRFT for mitigation of voltage sag, swell, harmonics and unbalance and their combinations in supply voltage[7]. The computer simulation results of SRFT based DVR are validated by using MATLAB/SIMULINK.

2. PRINCIPLE AND OPERATION OF DVR

The schematic diagram of three-phase, three-wire VSC based capacitor supported DVR is shown in Fig. 1 with three phase sources voltages (VMa, VMb, VMc) and three phase source series impedances (Zsa, Zsb, Zsc)[5]. The DVR uses a three phase transformer to inject voltage in series with supply voltage to maintain load voltage at rated value. A three-leg VSC along with a dc capacitor with dc link voltage (Vdc) is used in DVR. A series inductor (Lr) and a parallel capacitor (Cr) and resistor (Rr) are used to filter the harmonics in the injected voltages. In a capacitor-supported DVR, the power absorbed/supplied is zero under steady state condition and the voltage injected by the DVR is in quadrature with the feeder current[7]. The voltage injected by the DVR (Vca, Vcb, Vcc) is used to maintain the load voltages (VLa, VLb, VLc)) at the rated magnitude and this has two components, Vcad and Vcaq. The voltage in phase with current (Vcad) is to regulate the DC bus voltage and also to meet the power losses in the VSC of the DVR. The voltage in quadrature with the current (Vcaq) is to regulate the load voltage at a constant magnitude.

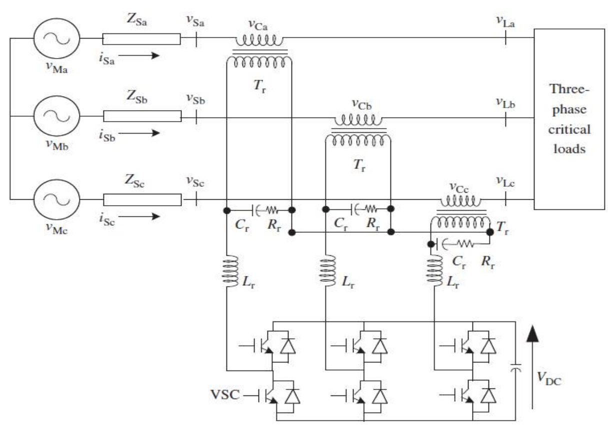

Fig. 1: Capacitor-supported DVR connected system

3. PROPOSED SRFT CONTROL ALGORITHM

The control algorithms for the DVR are based on the estimation of either injected voltages or thereference load voltages forpower quality improvement in a distribution system. The terminal voltages, source currents, load voltages, and the DC bus voltage are generally used as feedback signals and the reference load voltages are estimated using the control algorithms[6, 7]. There are many control algorithms reported in the literature for the control of DVR. In this paper control algorithm based on SRF theory is proposed. The basic principle of control algorithm with necessary mathematical expressions is discussed here.

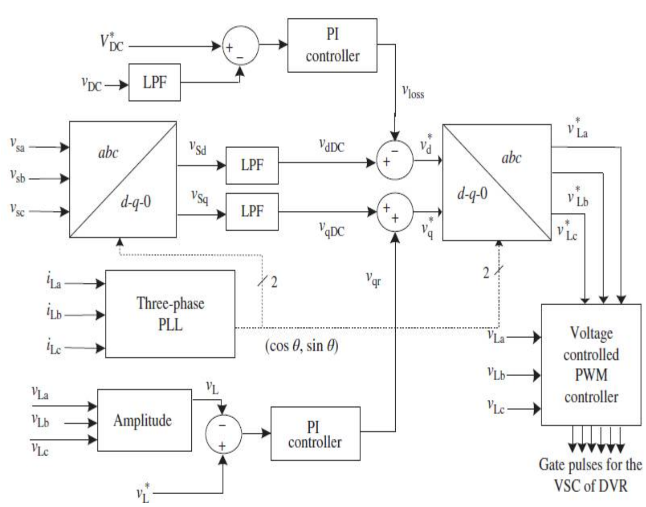

Fig. 2: Synchronous reference frame (SRF) theory-based method for control of self-supported DVR

The voltages at PCC (Vs) are converted to the rotating reference frame using the abc–dq0 conversion using the Park's transformation. The harmonics and the oscillatory components of the voltages are eliminated using low-pass filters (LPFs)[7].

The components of voltages in d- and q-axes are:

$$VSd = VdDC + VdAC \quad (1)$$

$$VSq = VqDC + VqAC(2)$$

The compensating strategy for compensation of voltage quality problems considers that the loadterminal voltage should be of rated magnitude and undistorted in nature. In order to maintain the DC bus voltage of the self-supported capacitor, a PI controller is used at the DC bus voltage of the DVR and the output is considered as the voltage loss (Vloss).

The reference d-axis load voltage is given as:

$$V^*d = VdDC - Vloss \quad (3)$$

The amplitude of the load terminal voltage (VL) is controlled to its reference voltage (V*L) using another PI controller. The output of PI controller is considered as the reactive component of voltage (Vqr) for voltage regulation of load terminal voltage. The amplitude of the load voltage (VL) at PCC is calculated from the AC voltages (VLa, VLb, VLc) as in Equation 4 .

$$VL=(2/3)^{1/2}\ (VLa^2 + VLb^2 + VLc^2)^{1/2}(4)$$

The reference quadrature axis load voltage is given as:

$$V^*q = VqDC + Vqr(5)$$

The reference load voltages (V*La, V*Lb, V*Lc) in abc frame are obtained from the reverse Park's transformation. The errors between the sensed load voltages (VLa, VLb, VLc) and reference load voltages are used in the PWM controller to generate gate pulses for the VSC of the DVR.

4. SIMULATION RESULTS

The performance of SRFT based Control Algorithm for three-phase, three-wire capacitor-supported VSC based DVR under various power quality disturbances are studied. The proposed capacitor-supported DVR is tested for various power quality disturbances like voltage sag, voltage swell, harmonics in supply voltage, unbalance source voltage and their combinations.

a) Performance of DVR during balanced voltage sag:

At the time interval of 2sec voltage sag of 15% is given in the supply side for 0. 1secs which is seen to be compensated by DVR in load side voltage in Fig. 3.

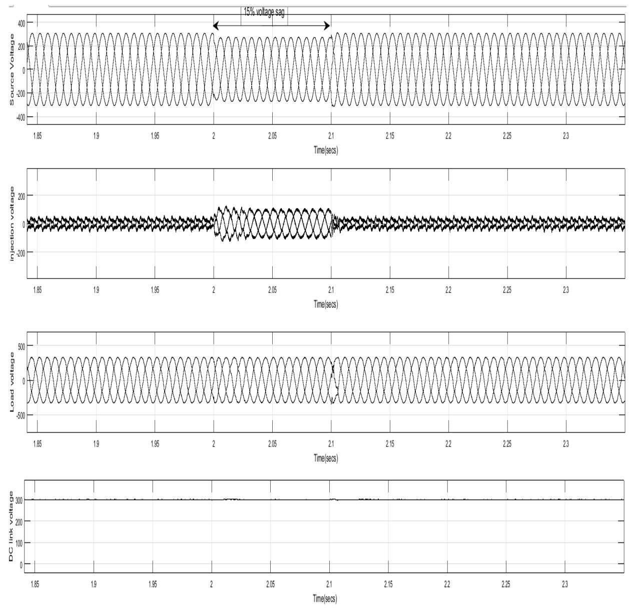

Fig. 3: DVR performance during balanced voltage sag

b) Performance of DVR during balanced voltage swell:

At the time interval of 2sec voltage swell of 15% is given in the supply side for 0. 1secs which is seen to be compensated by DVR in load side voltage in Fig. 4.

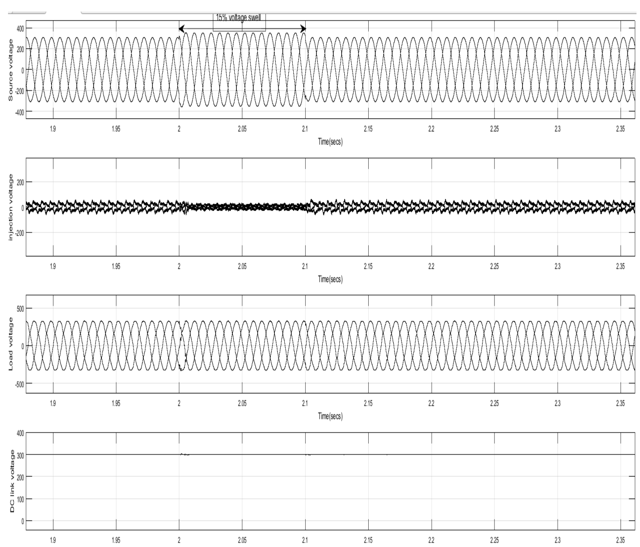

Fig. 4: DVR performance during balanced voltage swell

c) Performance of DVR during unbalanced voltage sag:
At the time interval of 2sec unbalanced voltage sag is given in the supply side for 0. 1secs which is seen to be compensated by DVR in load side voltage in Fig. 5

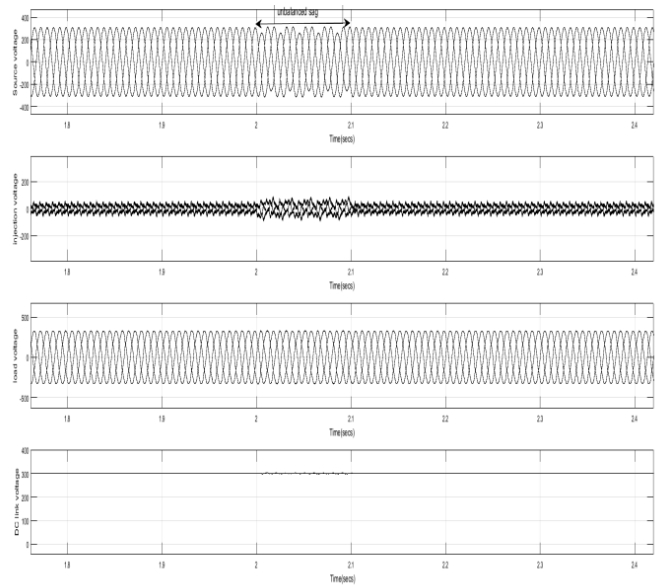

Fig. 5: DVR performance during unbalanced voltage sag

d) Performance of DVR during unbalanced voltage swell:
At time interval 2sec , unbalanced voltage swell is given in the supply side for 0. 1secs which is seen to be compensated by DVR in load side voltage in Fig. 6

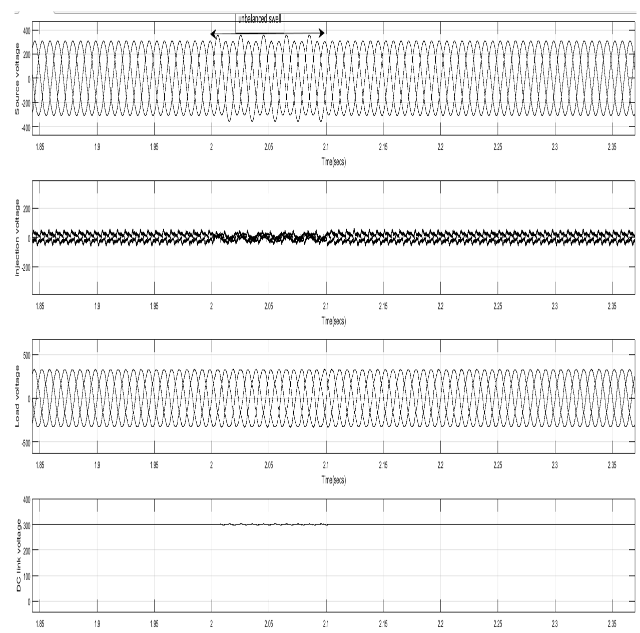

Fig. 6: DVR performance during unbalanced voltage swell

Performance of DVR during supply voltage harmonics:

Harmonics are introduced in the supply side voltage which is seen to be compensated by DVR in load side voltage in Fig. 7

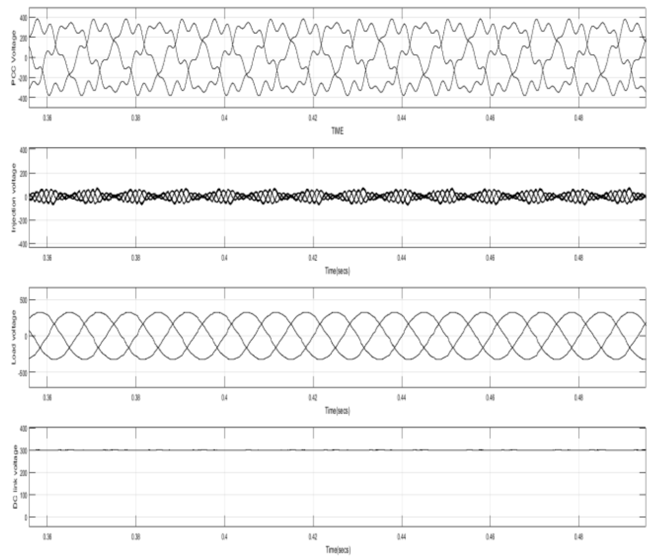

Fig. 7: DVR performance during supply voltage harmonics.

e) Performance of DVR during unbalanced voltage sag and voltage harmonic:

At an interval of 0. 4secs an unbalanced voltage is given for 0. 1 sec with harmonics in supply voltage and is seen both sag as well as harmonics being compensated in load voltage in Fig. 8.

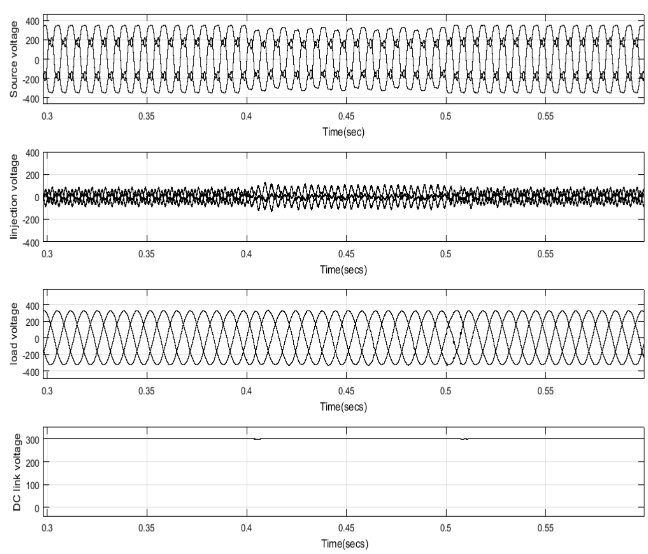

Fig. 8: DVR performance during supply voltage harmonics and unbalanced sag.

f) Performance of DVR during unbalanced voltage swell and voltge harmonics:

At an interval of 0. 6secs an unbalanced voltage is given for 0. 1 sec with harmonics in supply voltage and is seen both swell as well as harmonics being compensated in load voltage in Fig. 9.

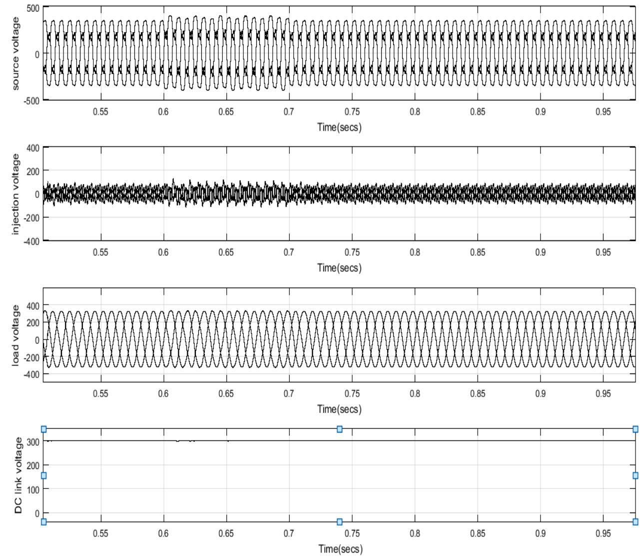

Fig. 9: DVR performance during supply voltage harmonics and unbalanced swell.

g) Comparison between THD of PCC voltage and of load voltage during harmonic compensation:

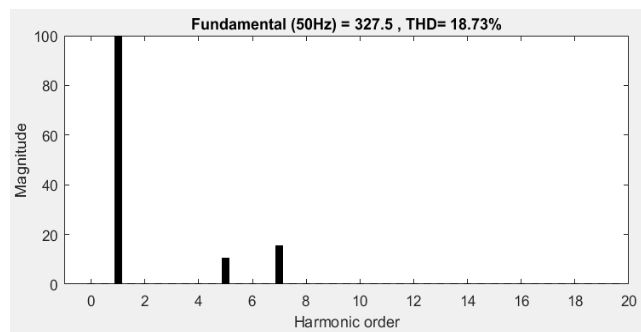

Fig. 10: THD of PCC voltage

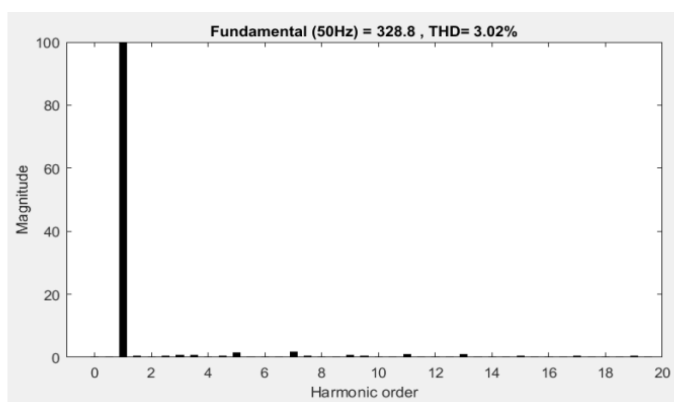

Fig. 11: THD of load voltage

5. CONCLUSION

The dynamic performance of SRFT control algorithm based DVR shows satisfactory results for mitigation of voltage sag, voltage swell, unbalanced source voltages and compensation of voltage harmonics. The results show that SRFT control algorithm based DVR is simple and robust to mitigate power quality problems related voltage. It was observed that sensed DC bus voltage (Vdc) is maintained at a reference value of 300V and sensed terminal voltage (Vt) is maintained at reference value of 327V during voltage sag, voltage swell, unbalanced source voltages and compensated voltage harmonics. The proposed SRFT control algorithm based DVR during harmonic compensation the load voltage (VL) has a THD of 3. 02%, source voltage (Vs) has a THD of 18. 73%, within IEEE-519 standard.

6. ACKNOWLEDGEMENT

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